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IMPROVING A GRID INVERTER WITH AN LCL OUTPUT FILTER FOR A PHOTOVOLTAIC ELECTRIC POWER SYSTEM OF OBJECT WHICH IS CONNECTED TO THE GRID

Abstract: *The issues of ensuring compliance with the requirements of IEC standards of current quality at the point of common coupling of a local object with a photovoltaic system to an AC grid are considered. Wherein non-sinusoidality of grid voltage and non-linear loads of the object in case of use of multifunctional grid inverter are taken into account. The structure of the inverter output filter is improved and its parameters are justified. The possibility of coordination it with the grid parameters is shown. It allows to increase the compensation efficiency of higher harmonics of the filter capacitor current at the point of common coupling to the grid. The structure of the control system has been improved with the introduction of current coupling of the filter capacitor into the channel of the inverter current reference forming. A model of the system "grid – inverter – load" for researching processes in the system is developed.*

Keywords: *combined electric power supply system, photovoltaic battery, converter unit, grid inverter, current control loop, THD, simulation.*

Problem statement

For local objects (cottages, motels, convenience stores, small businesses and agricultural facilities) with renewable energy sources (RES), a combined electric power systems (EPS) with connection to 0.4 kV AC distribution grid (DG) are widely used. In EPS the load of the local object and the output of the converter unit (CU) of the RES are connected to the DG and form a point common coupling (PCC). Wherein THD of DG current i_g (THDi_g) in PCC according to IEC standards for objects with distributed generation sources [1, 2] should not exceed 5%. On the other hand, standard [3] is valid in terms of voltage quality u_g for DG of general purpose, which assumes voltage non-sinusoidality (THD$u_g \leq 8\%$) and normalizes its harmonic composition (to 40th harmonic). And here there is a certain contradiction, which needs to be solved, since this cannot not affect on the quality of the current i_g. So, with the active load of the object in the case, when THD$u_g = 8\%$ we have THD$i_g = 8\%$ for current. In the case of active-inductive load with $\cos\varphi = 0.9$ in the presence in voltage u_g only 3rd and 5th harmonics with amplitudes according to [3] we have THD$u_g = 7.81\%$ and current THD$i_g = 4.05\%$. In the presence of non-linear load (rectifiers in household appliances, office equipment, industrial equipment, also led lighting systems) higher harmonics are generated in the DG current. So, the issue arises of exclusion of higher harmonics of current in PCC. A perspective solution of the problem is the use of multifunctional grid inverters in the CU [4-11] with combining the function of an active power filter (APF). It provides a power factor closed to 1 in the PCC while limiting the higher harmonics of the current and using the CU around the clock and other functions [7].

Analysis of the previous research

The combination of the grid voltage inverter (VSI) function of APF for compensation of influence the own load of object on DG in combined EPS is considered in [4-11]. However, the influence of non-sinusoidality of DG voltage is usually not taken into account, which leads to additional distortion of the load current of the object and affects on the setting of the current control loop (CCL), as well as on the determination the parameters of the power circuits of the grid inverter. Using of filter capacitor in PCC at non-sinusoidal voltage, it also causes the higher harmonics of DG current.

In work [9] output LCL – filter with a modulation frequency f_M = 6.8 kHz is being considered. Herewith for current values I_g = (0.005-1.0)I_{CMAX} in PCC THDi_g < 5% at VSI efficiency (η) on the level which is not lower than 0.97 (η is determined by the power loss in the switches of VSI). However, the use of large capacitance capacitor C_f = 60 μF in the output filter does not allow to ensure THDi_g < 5% at non-sinusoidal DG voltage. This is due to the higher harmonics of the filter capacitor current i_f [10, 11]. In principle, the capacitor can be excluded – we get L – filter of the first order. But then to suppress the current modulation harmonics of VSI should significantly (on order) to increase f_M, that is possible if MOSFET transistors use. Decrease of capacitor capacitance contributes to, but does not allow to obtain an acceptable THDi_g value. In works [10, 11] at the same time with a decrease of C_f the use of capacitor current compensation by inverter similarly that for the higher harmonics of the load current of a local object is proposed. Herewith the coupling by i_f is introduced to the forming reference current channel VSI. This raises the question of ensuring the stability of the system, since LCL – filter has a third order and phase shift –180° for higher harmonics. Respectively, we get a positive reverse current coupling on the current i_f. Therefore, a low-pass filter (LF) is introduced into the compensation channel with time constant $\tau = 10 \cdot 10^{-5}$ [10], a damping resistor R_f is introduced in series with the capacitor. Constant τ is large enough and the phase shift introduced by LF filter limits the possibilities of harmonics compensation. It allows only low-order harmonics (3rd, 5th, 7th) to be suppressed. Change the characteristics of the output filter is perspective for the improving of indicators of scheme thus, that it has properties closed to a first order filter (phase shift -90°) with effective suppression of modulation harmonics.

The aim of the study

Providing for the CU of the combined EPS of the local object compliance with the IEC standards current quality indicators in PCC in the whole range of its changes by improving the structure of the output filter and current control loop of grid VSI.

To achieve this aim, the following objectives are accomplished:

- to study the possibility of obtaining the desired characteristics of the output VSI filter;
- to develop the structure of power circles and control system that will provide compensation of higher harmonics at the point of connection to the grid;
- to develop a mathematical model on PC of the system: «DG - CU with PV - load».

Results of research

Consider the structure of single-phase CU (Fig. 1), containing: bridge VSI and photovoltaic solar battery PV with voltage converter (PV + DC/DC), that supports a set voltage value U at the entrance of VSI. DC link voltage is $U = aU_{gm}$ (a > 1) [9]. VSI is connected to DG with voltage $u_1 = U_{1m}\sin\omega t$ (U_{1m} – DG voltage amplitude, $\omega = 2\pi f$ – angular frequency, f = 50 Hz) and load. The load is active-inductive and nonlinear (uncontrolled rectifier).

To suppress higher harmonics in PCC LCL – filter is used. Appropriate sensors are provided for measuring currents and voltages.

The inductance (L_g) and DG active resistance (R_g) must be taken into account when determining the structure and parameters of the filter. Load resistance must be considered too.

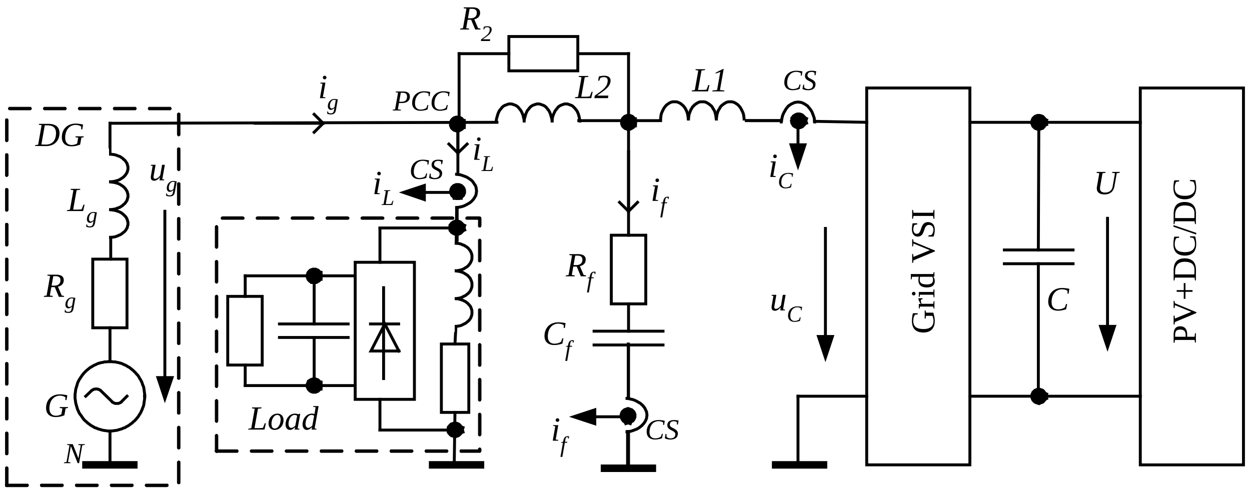

***FIGURE 1.** The structure of the power curcuits of the single-phase CU of combined EPS*

The basic element of the filter is the output reactor L_1 of VSI (consider reactor inductance unchanged). It's inductance L_1 determines the maximum value of the pulsation amplitude ΔI_{CMAX} of output VSI current i_C, which in unipolar modulation [9]

$$\Delta I_{Cm} = \Delta I_{CmMAX} = \frac{aU_{gm}}{16Lf_M}$$

where f_M is modulation frequency.

Value ΔI_{CMAX} is independent of current value i_C.

Inductance of the VSI reactor, proceeding from relative voltage of the DG reactor voltage value U_L (by the first harmonic) for maximum current of VSI I_{CMAX} (effective value)

$$L = \frac{bU_{gm}}{\omega\sqrt{2}I_{CmMAX}}$$

where $b = \frac{U_L}{U_g} = \frac{\omega L \cdot I_{CMAX}}{U_g}$ (U_g – effective voltage value of DG).

Modulation frequency according to [9, 10]

$$f_M \geq \frac{a\omega}{16bc} \tag{1}$$

where $c = \frac{\Delta I_{CmMAX}}{I_{CmMAX}}$.

If we accept the maximum value of the VSI output current I_{CMAX} = 25 A (I_{CmMAX} = 35.35 A), b = 0.15, c = 0.05, modulation frequency according (1) f_M = 3400 Hz, then ΔI_{CmMAX} = 1.77 A. Increase of f_M contributes to the reduction ΔI_{CMAX}, but leads to increasing energy losses in the VSI switches and these opportunities are limited. Value ΔI_{CMAX} is independent of the VSI current amplitude and of current, that is forming in DG. So, if c = 5% regarding to the maximum current value, with a ten-fold decrease of current it will be unacceptable. Possible without deterioration in the efficiency of the VSI is to increase the frequency to 6.8-8 kHz. Therefore, it is necessary to provide additional suppression of higher harmonics that is why usually used LCL – filter. With a sufficiently large inductance of the grid for this it is enough to connect a capacitor C_f to the PCC with damping resistor R_f. However, in the presence of a compensating coupling by the current of the filter capacitor, this solution leads to system instability and it is unacceptable.

The proposed structure of the output filter (Fig. 2) contains an additional reactor L_2 with resistor R_2. If we neglect the active resistances of the circuit, the angular frequency of cutoff of the filter

$$\omega_P = \sqrt{\frac{L_1 + (L_2 + L_g)}{L_1 \cdot (L_2 + L_g) \cdot C_f}}$$

Analysis of the characteristics of the output filter was carried out using the EWB program. Wherein (Fig. 2) the transfer characteristic by input influence i_C and output i_g was considered.

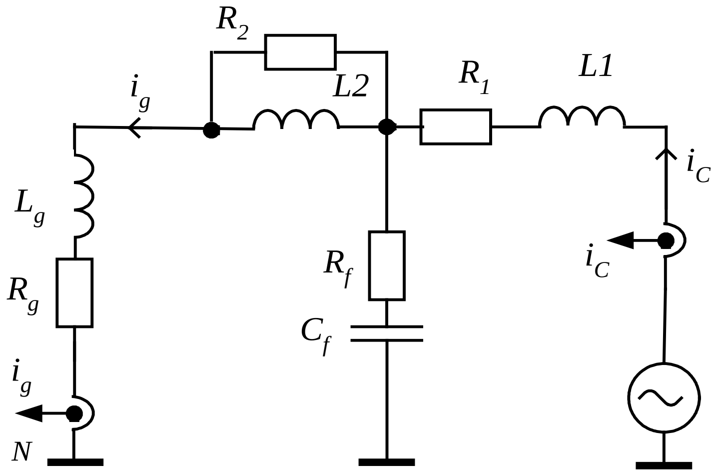

FIGURE 2. *Equivalent scheme of VSI output circuit*

So, at L_1 = 0.0042 H (b = 0.15), L_g = 0.00015 H, R_g = 0.1 Ohm, R_1 = 0.1 Ohm, C_f = 10 μF acceptable Bode diagrams (amplitude and phase-frequency characteristics) of filter (Fig. 3) are achieved when L_2 = 0.0003 H, R_2 = 4 Ohm, R_f = 2 Ohm. In this case, the cutoff frequency f_p = 2.497 kHz (transfer coefficient 2.3 dB or K = 1.3) for equivalent modulation frequency $f_{ME} = 2f_M = 2 \cdot 8$ = 16 kHz attenuation is 19.1 dB.

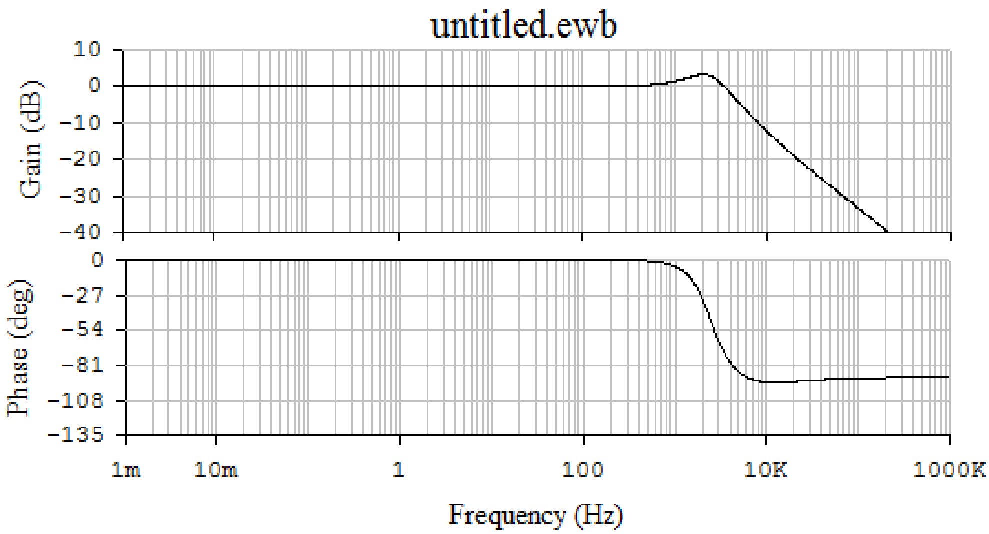

FIGURE 3. *Bode diagrams (amplitude and phase-frequency characteristics) of output filter*

Grid inductance L_g may be different. For coordination the filter characteristics, it is sufficient to change the resistor resistance value R_2. So, if L_g = 0.00005 H (less than three times) R_2 should be reduced three times too. Sure, the filter cutoff frequency will increase and the suppression of modulation current harmonics will worsen. With a larger value L_g should increase the value R_2 proportionally.

Decrease in phase shift introduced by the output filter to 90° provides stability of the VSI current control loop. Thus, it is possible to reduce the filter time constant in the current compensation circuit of the filter capacitor (LF), which provides suppression of modulation current harmonics and increase the efficiency of higher harmonic suppression i_f. So with τ = 5·10[-5] (cutoff frequency 3183.099 Hz) phase shift for 13th harmonic is about 11°.

Control system structure

VSI current set block structure and current control loop (Fig. 4) contains: adders, proportional link with coefficient k, integrating link $\frac{g}{p}$, dynamic compensation link DK ($\frac{L_1}{J}p$, $j = U / u_{TPm}$), multiplier block, PWM block with control pulse distributor of VSI switches, generator of modulating voltage GMV u_{TP} (has a triangular shape and is symmetrical about zero), phase locked loop PLL, low pass filter LF, phase shift compensation node of the current signal $C_f\ \delta\cos\omega t$ ($\delta = U_{gm}\omega C_f$). PWM by comparing the signal level from the output of the proportional link and u_{TR} implements unipolar modulation (PWM) of VSI output voltage.

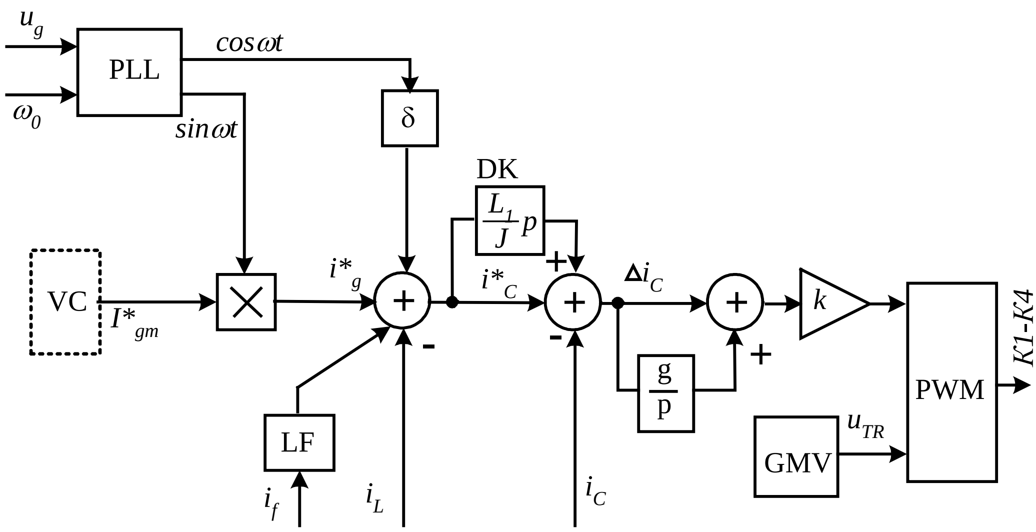

FIGURE 4. *Structure of block of current references of VSI and CCL*

Coefficient k of proportional link without taking into account the transmission coefficients of the sensors with a unit amplitude of the modulating voltage u_{TPm} = 1 according to [9, 10].

$$k \le \frac{1}{4 \cdot \Delta I_{CmMAX}}$$

Coefficient for integrating link is $g = \frac{f_M}{k}$.

According to the signal the amplitude reference of the grid current I^*_{gm} from output of external voltage controller VC (supports the voltage at the input of the VSI at a given level $U = U^*$) a sinusoidal signal of grid current i^*_{gm} reference is generated. The reference current of the grid VSI is determined taking into account the load current i_L, the capacitor current i_f, given via the LF and signal $\delta\cos\omega t$. PLL according DG voltage u_g and a given value of the angular frequency ω_0 forms signals $\sin\omega t$, $\cos\omega t$.

Simulation in Matlab and it's results

The structure of the model contains: DG, VSI with control system, DC source, imitating PV, and load. The load contains a constant non-linear load (uncontrolled rectifier with output capacitive filter and load power 900 W) and RL load. Total load power at $I_{Hm(1)}$ = 19.7 A, $\varphi_{(1)}$ = 27° is P_H = 2745 W and is about 0.5 from maximum VSI power. Model DG (220 V, f = 50 Hz) contains resistances R_g = 0.1 Ohm, L_g = 0.00015 H. Filter parameters L_1 = 0.0042 H, R_1 = 0.1 Ohm, R_f = 2 Ohm, C_f = 10 μF, L_2 = 0.0003 H, R_2 = 4 Ohm. A voltage-controlled source, the value of which is determined by the sum of harmonics of a given amplitude in accordance with [3], was used as source of alternative voltage. Grid VSI current is I_{CMAX} = 25 A (I_{CmMAX} = 35.35 A), f_M = 8 kHz. VSI input voltage according to [10, 11] U = 500 V (a = 1.6). The measurement of power losses in resistors R_2 and R_f are also provides for the model.

The operation of the system at sinusoidal and non-sinusoidal voltage DG is reviewed. To simplify the analysis, the operation of the CCL was considered and the grid current I^*_{gm} value was directly set. Values THDi_g evaluated by standard Matlab function taking into account all harmonics of current.

In Table 1 values THDi_{g3} are given in the presence of DG voltage of one harmonic with order n when using compensation by current i_f for value I^*_{1m} = 3 A and value THDi^*_{g3} in the absence of compensation. Also in Table 1 THDi^*_{g6} values are given for value I^*_{1m} = 6 A, which demonstrates the need for compensation also for large DG current values.

Table 1. *THDi_g in the presence of one harmonic $u_{g(n)}$*

n	1	11	13	17	19	21	23	25
$U_{g(n)}$, %	0	3.5	3	2	1.5	0.5	1.5	1.5
THDi_{g3}, %	4.05	4.19	4.49	4.64	4.72	3.83	5.43	6.01
THDi^*_{g3}, %		13.93	14.39	13.13	11.46	5.31	14.34	15.83
THDi^*_{g6}, %		6.97	7.18	6.57	5.73		7.13	7.93

Similar data are given in Table 2 for a combination of several harmonics of the voltage of the DG. The voltage harmonics of the DG were also set according to the standard [3].

Values of THDu_g in Table 2 exceed permissible standard [3] value. At values THDu_g closed to 8%, for example, n = 5 + 9 + 13 THDu_g = 7.04%, THDi_{g3} = 4.67%, THDi^*_{g3} = 18.1%. At n = 5 + 7 + 13 THDu_g = 8.38%, THDi_{g3} = 4.87%, THD$^*_{ig3}$ = 21.27%.

Table 2. *THDig with a combination of harmonics u_1*

n	3+5	3+…+7	3+..+9	3+….+11	3+..+13	3+…+17
THDu_g, %	7.81	9.28	9.51	10.03	10.69	10.68
THDi_{g3}, %	3.88	4.11	4.21	4.58	5.48	6.42
THDi^*_{g3}, %	11.75	16.77	17.38	22.01	26.08	28.98
by data [10]						
I^*_{gm}, A	2.8	3.2	3.2	4.2	5	7
THDi_g, %	4.79	4.67	4.85	4.91	4.96	4.74
THDi^*_g, %	12.78	15.76	16.31	15.63	15.42	12.33

To compare the effectiveness of the proposed solutions in Table 2 data from work [10] are given for I^*_{gm}, under which the condition $\mathrm{THD}i^*_g \leq 5\%$ is satisfied.

It has been established that for some combinations of harmonics of the mains voltage, the rate of change of the VSI current is insufficient for the CCL to work out the set current value. That is why the voltage at the input of the VSI should be increased to a = 1.7 (530 V).

Power losses in R_f do not exceed 2 W, in R_2 with a value I_{gm} = 35 A it is 2.8 W.

Voltage oscillograms of DG u_g, VSI u_C, currents DG i_g, VSI i_C, load i_L in the absence and presence of compensation at I^*_{gm} = 3 A are given in Figure 5.

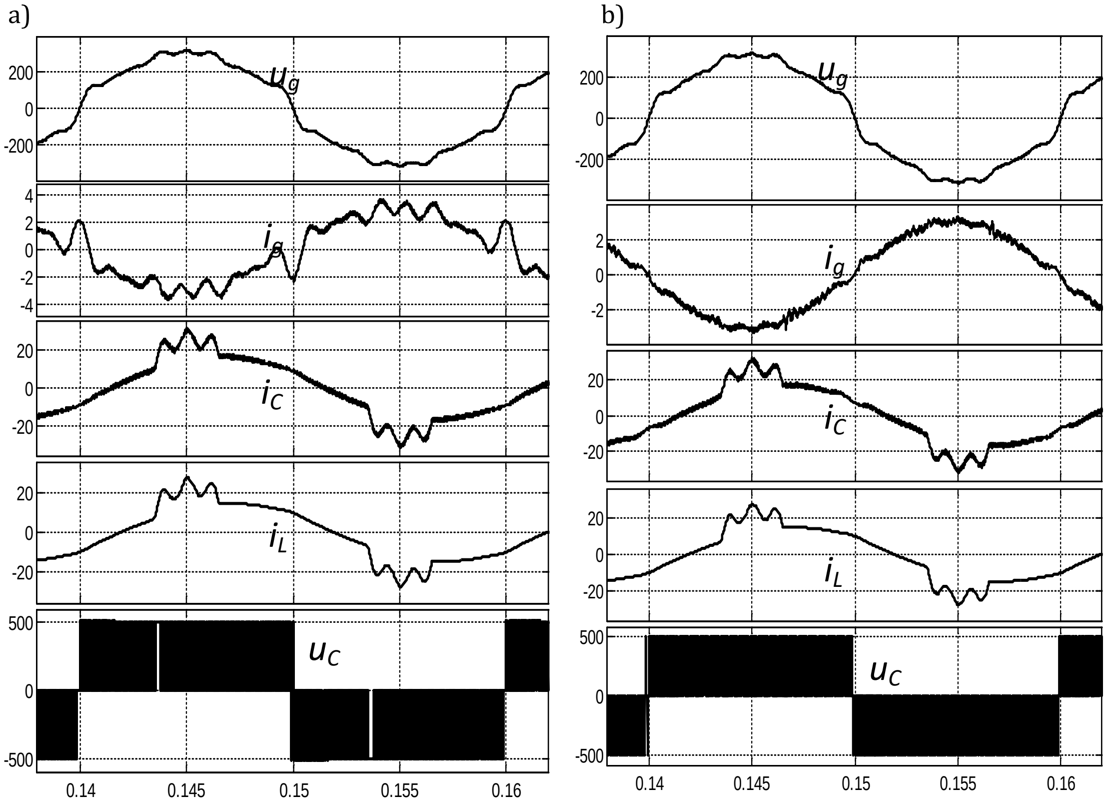

Figure 5. *Oscillograms of voltages and currents in the presence in voltage u_g (3rd +...+17th) harmonics: a) in the absence of compensation; b) in presence of compensation*

Evaluation of the possibility of using the output filter at constant values of inductances L_1, L_2 and at different inductance values L_g = 0.00005 H and L_g = 0.0003 H. At the same time resistance R_f was changed. The efficiency of harmonic compensation practically does not change. At reduction L_g value $\mathrm{THD}i_g$ increases due to an increase in modulation components of the current.

Conclusions

The presence of a capacitor in the PCC is necessary for the effective suppression of higher current harmonics while limiting the VSI modulation frequency. With a non-sinusoidal voltage DG, this leads to additional current harmonics. Using an LCL filter reduces capacitance and limits the generation of these harmonics. Given the compensating coupling of the capacitor current in the CCL, this allows $\mathrm{THD}i_g$ to comply with IEC standards. The weakness of the LCL filter is the gain increase in the region of the cutoff frequency and the phase shift of 180° for frequencies of large cutoff frequencies. When using compensating coupling, this leads to the threat of CCL stability loss. It is proposed to introduce an additional resistor into the filter, which allows reducing the phase shift to 90° with an acceptable deterioration in the suppression of higher harmonics. Reducing the threat of loss of stability creates the opportunity to reduce the filter time constant in compensating link for the capacitor current of the output filter. In combination with increasing the voltage at the input of the VSI, this provides compensation for the harmonics of the load current along with the harmonics of the filter current and allows you to maintain the value THD$i_g \leq 5\%$ in almost the entire range of variation of i_g values.

Based on the obtained solutions, a mathematical model is developed in Matlab for the system «DG – CU – load». The simulation results confirm the efficiency of the proposed solutions. A further area of research is the study of the possibilities of reducing energy losses in the power circuits of CU.

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